

**REMARKS**

Claims 25-32 have been amended and new claims 33-37 have been added. Accordingly, claims 25-37 are currently pending in the application. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

**Information Disclosure Statement**

This application is a continuation application of U.S. Serial No. 09/198,658, which has issued as U.S. Patent No. 6,205,556. Copies of all of the documents cited in the IDS were submitted during the prosecution of U.S. Serial No. 09/198,658. Therefore, pursuant to 37 CFR § 1.98(d), it is unnecessary to resubmit copies of those documents.

**Drawings**

Since this application is a continuation application of U.S. Serial No. 09/198,658, which has issued as U.S. Patent No. 6,205,556, the drawings 1-25 are not prior art.

**Abstract**

We have amended the abstract to comply with the proper format.

**Claim Rejections -35 USC 7 112**

Claims 29 and 30 stand rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth in the specification. This rejection is traversed as follows.

It is submitted that the first memory array and second memory array are adequately described in the specification, for example, on page 29, lines 25-30 and shown in Fig. 11. Furthermore, although the claims have been amended to change "a first signal path" and " a second signal path" to "a first bus" and "a second bus", respectively, we disagree that such a change is necessary. As shown in Fig.11, data lines, such as DA1,/DA1, which carry signals extend to the logic circuit, so "a first signal path coupled between said first memory array and said logic circuit" is adequately described. Also shown in Fig.11, read and write line pairs, OA,/OA,IA,/IA, which carry signals are coupled between the first memory array and the input/output circuit(I0). Thus, "a second signal path coupled between said first memory array and said input/output circuit"

is adequately described. Nonetheless, the wording has been changed to avoid any further delays in prosecution.

**Claim Rejections -35 USC 7 102(e)**

Claims 25-32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 4,988,891 to Mashiko (hereinafter "Mashiko"). This rejection is traversed as follows.

The semiconductor integrated circuit device, as recited in claim 25, has first and second modes. In the first mode, read and write operation to the memory array are performed. In the second mode, information is read from the memory array to the processing circuit. Also, during the first mode, a MOS transistor, which has a source/drain path between an arithmetic unit in the processing circuit and a power line, is in an OFF state. This allows for lower power consumption when the processing circuit is not carrying out operation.

Mashiko does not disclose or suggest two modes having features as in claim 25. Since the switching elements S1, S2, S3, S4 are each controlled by information stored in the random memory cells 150, 151, and output of an amplifier Ci, there is no disclosure of two modes as in claim 25. Also, Mashiko does not disclose or suggest a MOS transistor between an arithmetic

unit and a power line, which is in a OFF state during a mode when read and write operations are performed.

The semiconductor integrated circuit device, as recited in claim 29, includes a first bus coupled between the first memory array and the logic circuit; a second bus coupled between the logic circuit and the input/output circuit; and a third bus coupled between the first memory array and the input/output circuit. The semiconductor integrated device also has a first and second mode. In the first mode, by using the third bus, information from outside the semiconductor chip is written to the first memory array or information is read out of the semiconductor chip from the first memory array. In the second mode, by using the first bus, information is read from the first memory array to the logic circuit. By using the second bus, the logic circuit outputs results of the operation to the latch circuit. Also, by using the third bus, data in accordance with the results is written to the first memory array.

Mashiko does not disclose or suggest a second bus coupled between the logic circuit and input/output circuit. While Mashiko does disclose a bus coupled between switching elements and random memory cells 150, 151, and a bus coupled between random memory cells 150, 151 and interface(I/O), Mashiko does

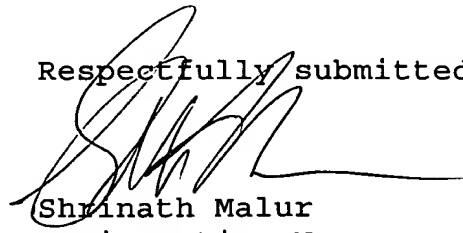
not disclose any separate bus for coupling the logic circuit and input/output circuit. Mashiko also does not disclose or suggest a first and second mode, as cited in claim 29.

Therefore, it is submitted that the rejection under 35 U.S.C. § 102(e) cannot be maintained. Furthermore, it is submitted that the pending claims are not obvious from the teaching of Mashiko. Thus, the pending claims patentably define the present invention over the cited art.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



Shrinath Malur  
Registration No. 34,663  
Attorney for Applicants

MATTINGLY, STANGER & MALUR  
1800 Diagonal Road, Suite 370  
Alexandria, Virginia 22314  
(703) 684-1120  
Date: July 10, 2003